

Appl. No. 10/666,570  
**Dated 04/05/2005**  
 Reply to Office Action of 01/05/2005

IN THE CLAIMS

Please amend claims 14 and 16 as follows below.  
 Please add new claims 33-37 as follows below.

MARKED UP CLAIMS LISTING

1           1-13. (Cancelled)

1           14. (Currently Amended) An instruction set architecture  
 2 (ISA) for execution of operations within a digital signal  
 3 processor to convert voice and data samples into packets for  
 4 transmission over a network and to convert packets received  
 5 from the network into voice and data samples, the instruction  
 6 set architecture comprising:

7                 a set of instructions for operation within a  
 8 digital signal processor wherein each instruction  
 9 includes a first operand accessed directly from memory,  
 10 a second operand accessed directly from memory of a  
 11 local register, and a destination register to store  
 12 results, the set of instructions including,

13                 a 20-bit DSP instruction, and  
 14                 a 40-bit DSP instruction,  
 15                 the set of instructions to accelerate  
 16 calculations within the digital signal processor of  
 17 the type where  $D = [ (A \text{ operation one } B) \text{ operation}$

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18                   two C } where operation one and operation two are  
19                   separate signal processing operations.

1           15. (Previously Presented) The instruction set  
2   architecture (ISA) of claim 14 for execution of operations  
3   within a digital signal processor, wherein,  
4           the twenty bit instruction uses mode bits in control  
5   registers and the forty bit instruction has a control  
6   extension to override the mode bits.

1           16. (Currently Amended) An instruction set architecture  
2   (ISA) for execution of operations within a digital signal  
3   processor to convert voice and data samples into packets for  
4   transmission over a network and to convert packets received  
5   from the network into voice and data samples, the instruction  
6   set architecture comprising:

7                   a set of instructions for operation within a  
8                   digital signal processor wherein each instruction  
9                   includes a first operand accessed directly from memory,  
10                  a second operand accessed directly from memory of a  
11                  local register, and a destination register to store  
12                  results, the set of instructions including,  
13                   a 20-bit DSP instruction,  
14                   a 40-bit DSP instruction, and

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15                   a dyadic instruction to execute two operations  
16                   in one instruction;  
17                   the set of instructions to accelerate  
18                   calculations within the digital signal processor of the  
19                   type where  $D = [ (A \text{ operation one } B) \text{ operation two } C ]$   
20                   where operation one and operation two are separate  
21                   signal processing operations.

1           17. (Original) The instruction set architecture (ISA)  
2   of claim 16 for execution of operations within a digital  
3   signal processor, wherein  
4           the two operations of the dyadic instruction for  
5   execution in one instruction are DSP operations.

1           18. (Original) The instruction set architecture (ISA)  
2   of claim 17 for execution of operations within a digital  
3   signal processor, wherein  
4           the DSP operations are of the set of operations of  
5   multiplication, addition, extremum, and no operation.

1           19-20. (Cancelled)

1           21. (Previously Presented) The instruction set  
2   architecture (ISA) of claim 15 for execution of operations  
3   within a digital signal processor, wherein,

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4           the control registers are mode registers.

1           22-29. (Cancelled)

1           30. (Previously Presented) The instruction set  
2 architecture (ISA) of claim 14 for execution of operations  
3 within a digital signal processor, wherein  
4           the digital signal processing operations are of the set  
5 of operations of multiplication, addition, extremum, and no  
6 operation.

1           31. (Previously Presented) The instruction set  
2 architecture (ISA) of claim 16 for execution of operations  
3 within a digital signal processor, wherein,  
4           the twenty bit instruction uses mode bits in control  
5 registers and the forty bit instruction has a control  
6 extension to override the mode bits.

1           32. (Previously Presented) The instruction set  
2 architecture (ISA) of claim 31 for execution of operations  
3 within a digital signal processor, wherein,  
4           the control registers are mode registers.

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1           33. (New) An instruction set architecture (ISA) for  
2 voice over internet protocol (VOIP), the instruction set  
3 architecture comprising:  
4                 a set of instructions for operation within a  
5                 digital signal processor to convert between samples and  
6                 packets for voice and data communication over a  
7                 network, wherein each instruction includes a first  
8                 operand accessed directly from memory, a second operand  
9                 accessed directly from memory of a local register, and  
10                a destination register to store results, the set of  
11                instructions including,  
12                         a 20-bit DSP instruction, and  
13                         a 40-bit DSP instruction,  
14                         the set of instructions to accelerate  
15                calculations within the digital signal processor of  
16                the type where  $D = [ (A \text{ operation one } B) \text{ operation}$   
17                two  $C ]$  where operation one and operation two are  
18                separate signal processing operations.

1           34. (New) The instruction set architecture (ISA) of  
2 claim 33, wherein  
3                 the twenty bit instruction uses mode bits in control  
4                 registers and the forty bit instruction has a control  
5                 extension to override the mode bits.

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1           35. (New) The instruction set architecture (ISA) of  
2 claim 33, wherein  
3           the digital signal processing operations are of the set  
4 of operations of multiplication, addition, extremum, and no  
5 operation.

1           36. (New) The instruction set architecture (ISA) of  
2 claim 35, wherein,  
3           the twenty bit instruction uses mode bits in control  
4 registers and the forty bit instruction has a control  
5 extension to override the mode bits.

1           37. (New) The instruction set architecture (ISA) of  
2 claim 36 for execution of operations within a digital signal  
3 processor, wherein,  
4           the control registers are mode registers.